Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	via and trench and (semiconductor adj material) and (crystallization or crystallizing) and Infineon	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/18 09:09
L2	294	via and trench and (semiconductor adj material) and (crystallization or crystallizing)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/18 10:41
L3	238	2 and @ad<"20030923"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/18 10:38
L4	56	2 not 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/18 09:31
L5	1	("20020074566").PN.	US-PGPUB; USPAT	OR	OFF	2005/10/18 10:37
L6	1646	438/268,269,270,589,272.ccls.	US-PGPUB; USPAT	OR	ON	2005/10/18 10:38
L7	238	2 and @ad<"20030923"	US-PGPUB; USPAT	OR	ON	2005/10/18 10:38
L9	6	(via and (trench or opening or recess or groove or hole or aperture) and (semiconductor adj material) and (crystallization or crystallizing)).clm.	US-PGPUB; USPAT	OR	ON	2005/10/18 10:42

US-PAT-NO: 6756277

DOCUMENT-IDENTIFIER: US 6756277 B1
See image for Certificate of Correction

TITLE: Replacement gate process for transistors having elevated source and drain regions

---------- KWIC ---------

Claims Text - CLTX (1):

1. A method of manufacturing an integrated circuit, the integrated circuit including a gate structure on a substrate, the substrate including a shallow source extension and a shallow drain extension, the gate structure including a gate conductor above a high-k gate dielectric layer, the method comprising steps of: providing a mask structure above the high-k gate dielectric layer on the substrate; etching the high-k gate dielectric layer in accordance with the mask structure; providing spacers on sidewalls of the mask structure; removing the mask structure thereby leaving an **aperture** between the spacers; providing an amorphous semiconductor layer above the substrate, the amorphous semiconductor layer filling the **aperture** and having a top surface higher than a top of the spacers; removing the amorphous semiconductor layer to expose the top of the spacers; and forming a single crystalline **semiconductor material** at an elevated source and an elevated drain location from the amorphous semiconductor layer **via** a solid phase epitaxy process.

Claims Text - CLTX (10):

10. A method of manufacturing an ultra-large scale integrated circuit including a transistor, the method comprising: providing a gate structure on a top surface of a substrate, the gate structure including a sacrificial structure and a high-k gate dielectric: providing a pair of spacers for the gate structure; removing the sacrificial structure to form an **aperture** between the spacers; depositing an amorphous **semiconductor material** above the top surface of the substrate, the amorphous **semiconductor material** filling the **aperture** and covering the spacers; removing a portion of the amorphous **semiconductor material** so that the amorphous **semiconductor material in the aperture** is separated from the amorphous material above the top surface of the substrate by the spacers; and **crystallizing** the amorphous **semiconductor material** in an annealing process.

Claims Text - CLTX (12):

12. The method of claim 11, further comprising: polishing the amorphous **semiconductor material** before the a **crystallizing** step.

Claims Text - CLTX (17):

17. A process of forming a transistor with elevated source and drain regions, the process comprising: providing a gate structure having a sacrificial structure and a high-k gate dielectric, the high-k gate dielectric being disposed above a substrate; providing a spacer structure for the gate structure; removing the sacrificial structure; depositing an amorphous **semiconductor material** above the substrate and the spacer structure, the amorphous **semiconductor material** covering the spacer structure, the amorphous **semiconductor material** replacing the sacrificial structure; removing the amorphous **semiconductor material** to expose the spacer structure; and **crystallizing** the amorphous **semiconductor material** to form single crystalline material.